WHAT IS CLAIMED IS:

1. A low-capacitance bonding pad structure for a semiconductor device, the structure comprising:

a substrate;

a stacked metal layer positioned on the substrate, wherein the stacked metal layer further comprises a plurality of metal layers and a plurality of dielectric layers, which are alternately stacked up, and the metal layers are coupled by a plurality of via plugs in the dielectric layers;

an uppermost metal layer positioned on the stacked metal layer, wherein an area of each metal layer in the stacked metal layer is smaller than that of the uppermost metal layer; and

a passivation layer having a bonding pad opening positioned on the uppermost metal layer, wherein the bonding pad opening exposes a portion of the uppermost metal layer.

2. The structure of claim 1, wherein the metal layers in the stacked metal layer are in the shape of bars.

3. The structure of claim 2, wherein the bar direction of each layer of the metal layers is across to each other for the different metal layers.

4. The structure of claim 2, wherein the metal layers are stacked and aligned with each other.

5. The structure of claim 1, wherein the metal layers in the stacked metal layer comprises concentric polygons.

6. The structure of claim 1, wherein the metal layers in the stacked metal layer comprises concentric circles.

7. The structure of claim 1, wherein the metal layers in the stacked metal layer comprises a mesh structure.

8. The structure of claim 7, wherein the metal layers in the stacked metal layer are aligned with each other.

9. The structure of claim 7, wherein the mesh is composed of a unit geometric shape.

10. The structure of claim 9, wherein the unit shape is a polygon.

11. The structure of claim 9, wherein the unit shape is a circle.

12. The structure of claim 1, wherein the mesh is composed of various unit shapes.

13. The structure of claim 1, wherein locations of the via plugs in two adjacent layers of the dielectric layers are shifted with a proper distance.

14. A semiconductor structure, the structure comprising:

a substrate;

a bonding pad over the substrate, wherein the bonding pad comprises a stacked metal layer and an uppermost metal layer; and

a device located on the substrate just under the bonding pad.

15. The structure of claim 14, wherein the stacked metal layer comprises a plurality of metal layers and a plurality of dielectric layers, which are alternatingly stacked up, and the metal layers are coupled by a plurality of via plugs in the dielectric layers.

16. The structure of claim 14, wherein an area of each metal layer in the stacked metal layer is smaller than that of the uppermost metal layer.

17. The structure of claim 14, wherein the structure further comprises a signal line and a power line between the device and the bonding pad.

18. The structure of claim 17, wherein the stacked metal layer comprises a plurality of metal layers and a plurality of dielectric layers, which are alternatingly stacked up, and the metal layers are coupled by a plurality of via plugs in the dielectric layers.

19. The structure of claim 17, wherein an area of each metal layer in the stacked metal layer is smaller than that of the uppermost metal layer.

20. The structure of claim 14, wherein the device on the substrate just under the bonding pad is an active device.

21. The structure of claim 14, wherein the device on the substrate just under the bonding pad is a passive device.

22. A low-capacitance bonding pad structure for a semiconductor device, the structure comprising:

a substrate having a well;

a doped region as a diffusion region formed in the well; and

a bonding pad over the substrate and aligned with the doped region, wherein the bonding pad comprises a stacked metal layer and an uppermost metal layer.

23. The structure of claim 22, wherein ions doped in the doped region is opposite to those in the well.

24. The structure of claim 22, wherein the stacked metal layer comprises a plurality of metal layers and a plurality of dielectric layers, which are alternatingly stacked up, and the metal layers are coupled by a plurality of via plugs in the dielectric layers.

25. The structure of claim 22, wherein an area of each metal layer in the stacked metal layer is smaller than that of the uppermost metal layer.